

NSR10A1/2 Series

100V, 1A/2A, High Efficiency, Asynchronous Step-down Converter

Preliminary specifications subject to change without notice

Datasheet (EN) 0V5

Product Overview

The NSR10A1/2 series are asynchronous step-down DC-DC converters with wide input voltage ranging from 5.5V to 100V. This high voltage converters have an integrated 100V, 500mΩ N-channel buck switch. For NSR10A12 and NSR10A22 version, a 100mA LDO is integrated for two power-stage application with a 30V input voltage rating.

The NSR10A1/2 series have an inherent adaptive constant-on-time control with no control loop compensation required. The switching frequency works on a fixed 300kHz as on-time is proportion to duty ratio. Over-current protection is achieved by internal cycle-by-cycle 2A (NSR10A11/NSR10A12) and 4A (NSR10A21/NSR10A22) peak switching current limit. An inherent hiccup mode is designed for short circuit protection.

The NSR10A1/2 series operate in ambient temperatures from -40°C to 125°C. The devices are available in an 8-pin HSOP8 package.

Key Features

- Wide 5.5V to 100V Input Range
- Peak Switching Current Limit:
 - NSR10Ax1: 1A Current Capability with 2A Peak Current Limit
 - NSR10Ax2: 2A Current Capability with 4A Peak Current Limit
- Integrated 500mΩ High-Side Power MOSFETs
- Optional Integrated 30V/100mA (150mA Current Limit) LDO
- Adaptive Constant-on-time Control
- 300kHz Switching Frequency
- 1.2V $\pm$ 1.5% Feedback Reference Voltage
- 4ms Internal Soft-start Time
- No Control Loop Compensation Required
- Cycle-by-Cycle Current Limit
- Short circuit protection with hiccup mode

- Over-Voltage Protection
- Over-Temperature Protection

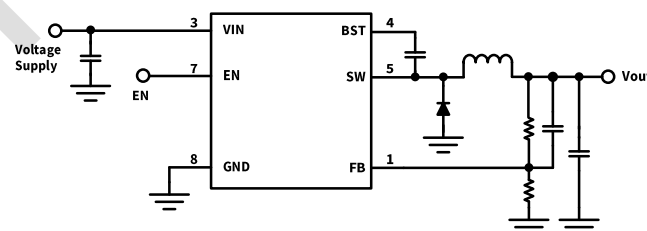
Applications

- E-bike, E-scooter
- Power Tools
- Moto Drives, Inverters
- Drones

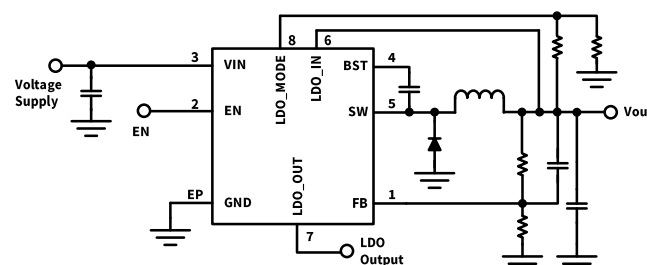
Device Information

Part Number	Version info	Package Info
NSR10A11	1A w/o LDO	3.90 mm × 4.90 mm HSOP8
NSR10A12	1A w/ LDO	3.90 mm × 4.90 mm HSOP8
NSR10A21	2A w/o LDO	3.90 mm × 4.90 mm HSOP8
NSR10A22	2A w/ LDO	3.90 mm × 4.90 mm HSOP8

Typical Application



NSR10A11/NSR10A21 Typical Application Circuit



NSR10A12/NSR10A22 Typical Application Circuit

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1. Pin Configuration and Functions

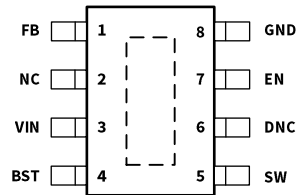


Figure 1. NSR10A11/NSR10A21 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	FB	Feedback input pin.
2	NC	Not internally connected.
3	VIN	Power supply pin.
4	BST	Boost bootstrap capacitor input. Connect a 0.1uF capacitor from BST pin to SW pin.
5	SW	Switching node pin.
6	DNC	Do not be connected externally.
7	EN	Enable pin, with internal pull-up current source. Float to enable.
8	GND	Ground reference.
EP	NC	Not internally connected.

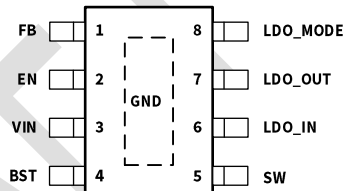


Figure 2. NSR10A12/NSR10A22 Pin Configuration

PIN NO.	SYMBOL	FUNCTION
1	FB	Feedback input pin.
2	EN	Enable pin, with internal pull-up current source. Float to enable.
3	VIN	Power supply pin.
4	BST	Boost bootstrap capacitor input. Connect a 0.1uF capacitor from BST pin to SW pin.
5	SW	Switching node pin.
6	LDO_IN	Internal LDO input.
7	LDO_OUT	Internal LDO output.

PIN NO.	SYMBOL	FUNCTION
8	LDO_MODE	LDO mode selection input. When LDO_MODE<0.2V, LDO is disabled, when LDO_MODE > VLDO_SEL, LDO_OUT is set to 5V, when VLDO_MODE < VLDO_SEL, LDO_OUT is set to 3.3V
EP	GND	Ground reference.

2. Absolute Maximum Ratings

Description	Min	Max	Units
VIN to GND	-0.3	105	V
BST to GND	-0.3	VIN + 6	V
SW to GND	-1	105	V
FB to GND	-0.3	6	V
BST to VCC		TBD	V
BST to SW		6	V
EN to GND	-0.3	6	V
LDO_IN to GND (NSR10A12/22 only)		30	V
LDO_MODE to GND (NSR10A12/22 only)	-0.3	6	V
LDO_OUT to GND (NSR10A12/22 only)	-0.3	6	V
Lead temperature (soldering 4 sec)		260	°C
Storage temperature	-55	150	°C

3. ESD Ratings

Description	Min	Max	Unit
Electrostatic discharge, Human-body model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2000	2000	V
Electrostatic discharge, Charged-device model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (2)	-500	500	V
Electrostatic discharge, Machine Model (MM)	-200	200	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	V _{IN}	5.5		100	V
Operating Junction Temperature	T _J	-40		125	°C

5. Thermal Information

Parameters	Symbol	SOP8-EP	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	39.6	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	7.9	°C/W

6. Specifications

6.1. Electrical Characteristics

($V_{IN}=48V$, $T_a=-40^{\circ}C$ to $125^{\circ}C$. Unless otherwise noted, typical value is at $T_a = 25^{\circ}C$.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
VIN/VCC						
VIN UVLO Threshold	VIN_UVLO	5.2	5.6	5.9	V	VIN Rising
VIN UVLO Threshold Hysteresis	VIN_UVLO_HYS		500		mV	
Quiescent Current	IQ		120		uA	Not switching
Shutdown Current	ISHD		5.2		uA	EN=0, no load
Driver/Power MOSFET/Current limit						
High-side Switch On-State Resistance	RDS(on)_HS		0.5		Ω	VBST-VSW=5V
Gate Drive UVLO (VBST-VSW)	VGATE_UV	2.7	3.2	4.9	V	Rising
Gate Drive UVLO Hysteresis	VGATE_UV_HYS		200		mV	
Breakdown Voltage, VIN to GND	VDS(max)	105			V	TJ = 25°C
		TBD			V	TJ = -40°C to 125°C
Breakdown Voltage, BST to VCC	VBST_VCC(max)	105			V	TJ = 25°C
		TBD			V	TJ = -40°C to 125°C
Current Limit Threshold	ICL	TBD	2	TBD	A	NSR10A11/12
		TBD	4	TBD	A	NSR10A21/22
Current Limit Response Time	tCL_RESP		225		ns	ISW overdrive = 0.1 A, time to switch off
Switching frequency	fSW		300		kHz	
FB/EN/Soft-start/Protection						
FB Reference Threshold	VREF	1.182	1.2	1.218	V	
FB Overvoltage Threshold	VOV_REF		115%			Trip point for switch OFF
FB Overvoltage Recovery Threshold	VOV_REC		111%			
FB Bias Current	IFB		100		nA	
Enable threshold	VEN	1.15	1.20	1.25	V	
Enable Hysteresis	VEN_HYS		200		mV	
Enable threshold	IEN		2.3		uA	EN=1.5V
Soft Start Time	TSS		4		ms	
Thermal Shutdown Temperature	TSHD		165		°C	

NSR10A1/2 Series

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Thermal Shutdown Hysteresis	THYS		25		°C	
Internal LDO						
LDO EN Threshold	VLDO_EN	TBD	0.2	TBD	V	
LDO EN Threshold Hysteresis	VLDO_EN_HYS		TBD		V	
LDO Select Threshold	VLDO_SEL	TBD	2	TBD	V	When VLDO_MODE > VLDO_SEL, LDO OUT = 5V, When VLDO_MODE < VLDO_SEL, LDO OUT = 3.3V
LDO Select Threshold Hysteresis	VLDO_SEL_HYS		TBD		V	
LDO Output Voltage	VLDO_OUT	4.9	5	5.1	V	VLDO_MODE > VLDO_SEL, ILDO from 1mA to 100mA
		3.25	3.3	3.35	V	VLDO_MODE < VLDO_SEL, ILDO from 1mA to 100mA
LDO Output current limit	ILDO_CL		150		mA	

6.2. Typical Performance Characteristics

TBD

7. Detailed Description

7.1. Overview

The NSR10A1/2 series are asynchronous step-down DC-DC converter with wide input voltage ranging from 5.5V to 100V which designed for a variety of step-down applications. This high voltage converters have an integrated 100-V, 500mΩ N-channel buck switch. For NSR10A12 and NSR10A22 version, a 100mA LDO is integrated for two power-stage application which has 30V input voltage rating. The devices are easy to implement and is provided in thermally enhanced SOP8-EP package.

The NSR10A1/2 series have an inherent adaptive constant-on-time control with no control loop compensation required. An internal ripple injection circuit brings benefits that there is no external ripple circuit needed nor an electrolytic capacitor with considerable equivalent series resistance (ESR). The switching frequency works on a fixed 300-kHz as on-time is proportion to duty ratio.

The NSR10A1/2 series have cycle-by-cycle 2A (NSR10A11/NSR10A12) and 4A (NSR10A21/NSR10A22) peak switching current limit current limit. An inherent hiccup mode is designed for short circuit protection. There is also an over-voltage-protection. The NSR10A1/2 series operate in ambient temperatures from -40°C to 125°C. The devices are available in an 8-pin SOP8-EP package.

7.2. Block Diagram

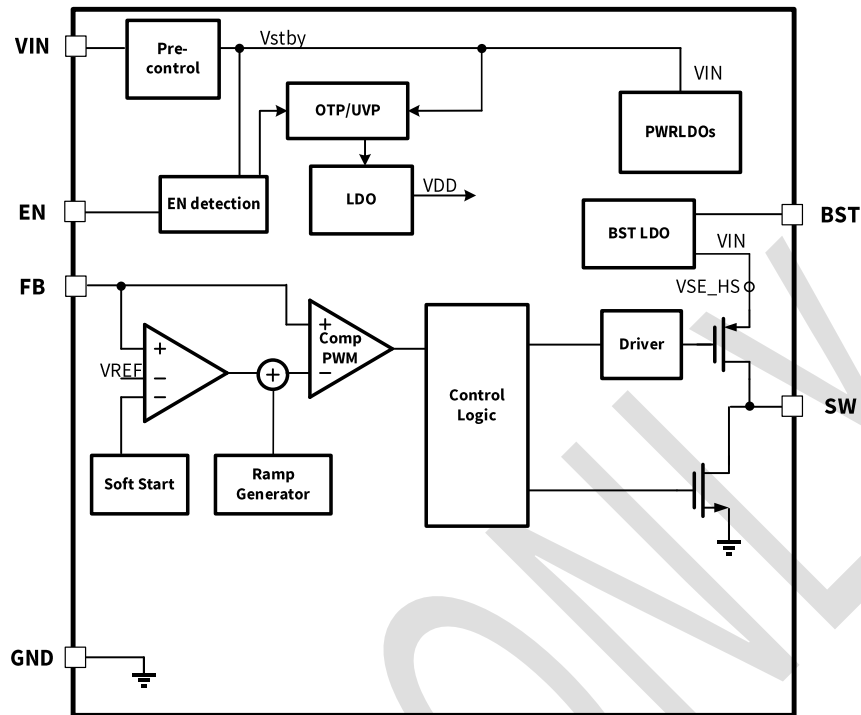


Figure 3 Block Diagram of NSR10A11/21

7.3. Feature Description

TBD

7.4. Typical Application

7.4.1. Application Circuit

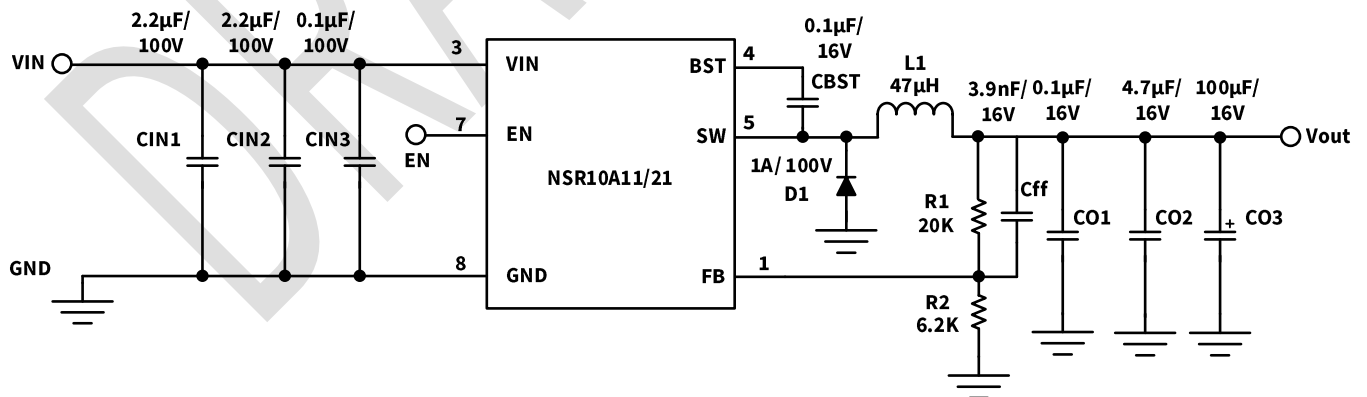


Figure 4 VIN=8 ~ 100V, VOUT=5V, IOUT=0 ~ 2A

NSR10A1/2 Series

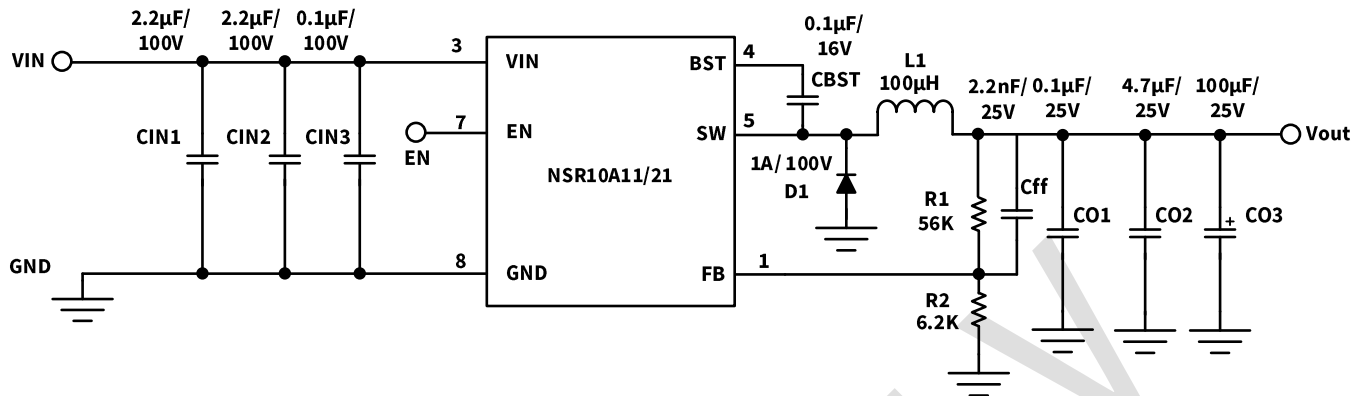


Figure 5 VIN=15 ~ 100V, VOUT=12V, IOUT=0 ~ 2A

8. Layout Example

8.1. Layout Guidelines

For input trace, capacitors should be close to IN pin and GND pin. For output trace, capacitors should be close to current path. Both input and output traces should be wide enough for rating current capability. For GND trace, large polygon plane should be used for better heat dissipation, via arrays are recommended connect multiple layers to improve thermal performance. For adjustable versions, feedback resistors should be close to FB pin. For SW node, inductor should close to the SW pin, to reduce radiated noise related to high dv/dt.

8.2. Layout Example

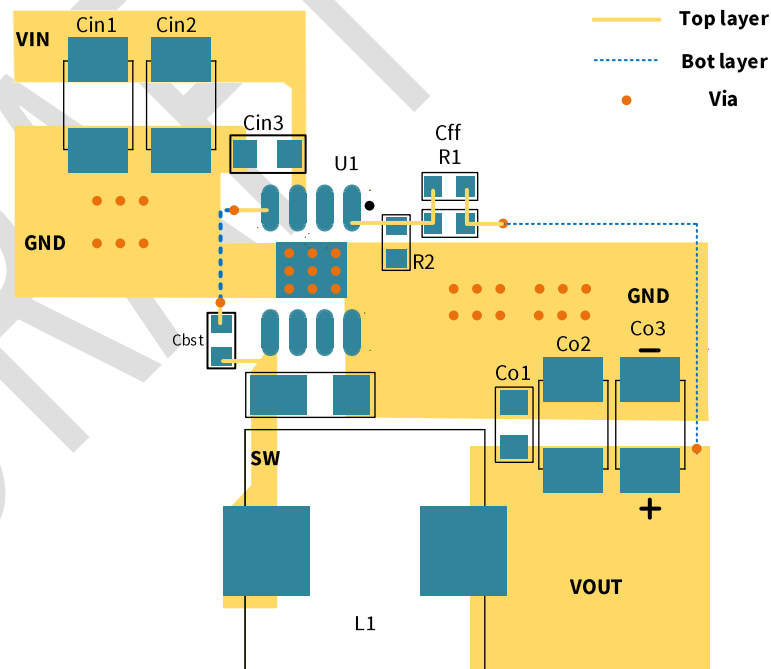


Figure 6 NSR10A11/A21 Layout Example

9. Package Information

9.1. Mechanical Data

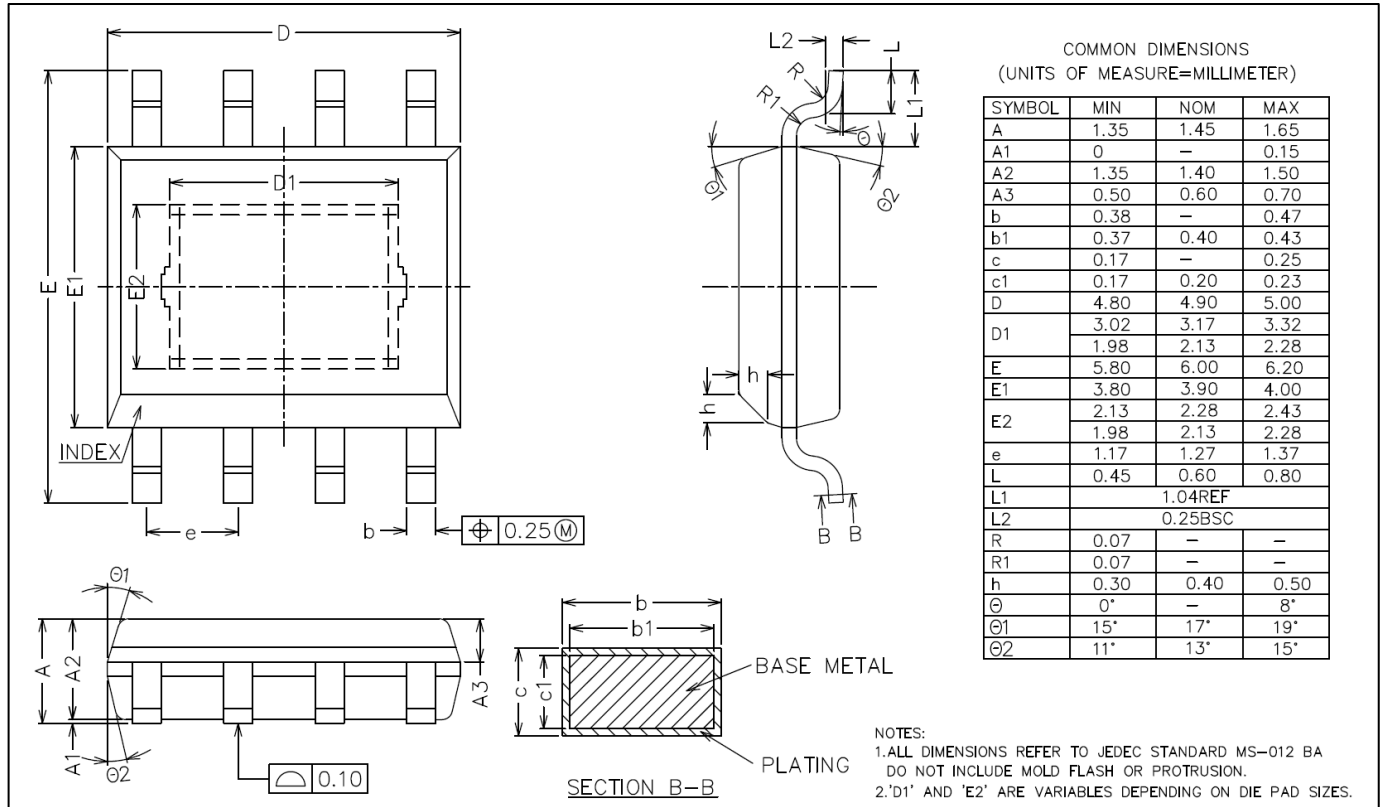


Figure 7 HSOP8 Package Information

9.2. Recommended Land Pattern

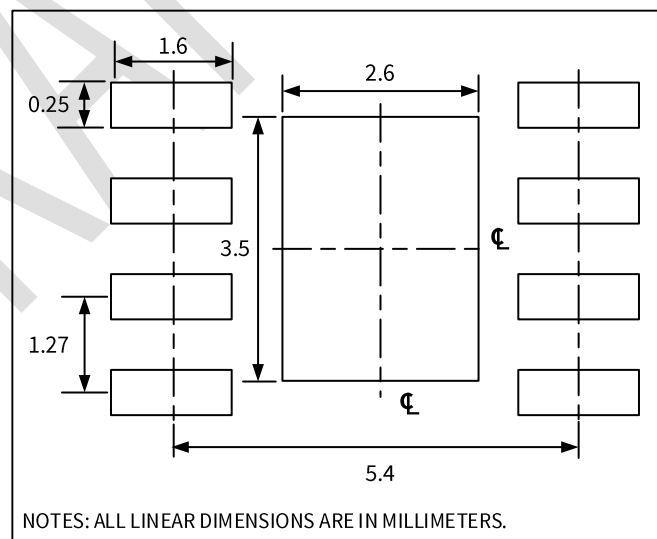


Figure 8 Recommended Land Pattern

10. Order Information

Orderable Part Number	MSL	Package	SPQ	Marking
NSR10A11-DHSPR	1	HSOP8	2500	10A11
NSR10A21-DHSPR	1	HSOP8	2500	10A21
NSR10A12-DHSPR	1	HSOP8	2500	10A12
NSR10A22-DHSPR	1	HSOP8	2500	10A22

11. Revision history

Revision	Description	Date
0V1	Initial version	2021/12
0V2	Spec updates	2022/03
0V3	Update IMPORTANT NOTICE & Device Information	2023/04
0V4	Update VIN range	2023/04
0V5	Update Package Information & Typical Application & etc.	2023/07

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