

Value line Triple-Channel Digital Isolators With Integrated DC to DC Converter

Datasheet (EN) 0.4

Product Overview

The NIRSP31 device is value line triple-channel digital isolators with integrated isolated DC-DC converter. The isolated DC-DC converter provide up to 300mW output power use on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NIRSP31 device is safety certified by UL1577 support 2kVrms insulations withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NIRSP31 is up to 20Mbps, and the common-mode transient immunity (CMTI) is up to 50kV/us. The NIRSP31 devices provide 5V to 5V, 5V to 3.3V conversion mode, the output voltage can be set by SEL pin.

Key Features

- Up to 2000V_{rms} Insulation voltage for NIRSP31
- Power supply voltage: 4.75V to 5.25V
- support 60mA load current
- Over current and over temperature protection
- Date rate: DC to 20Mbps
- High CMTI: 50kV/us
- Propagation delay: <50ns
- High system level EMC performance:
 - Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~105°C
- RoHS-compliant packages: LGA-18

Applications

- Industrial Battery Management System
- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation

Device Information

Part Number	Package	Body Size
NIRSP31-DLARR	LGA 18	4.00 × 5.00mm

Functional Block Diagrams

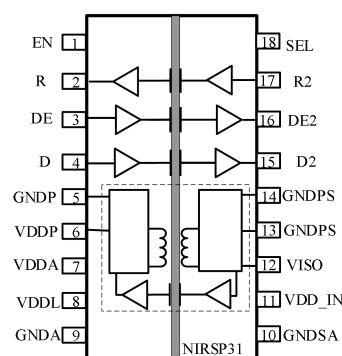


Figure 1. NIRSP31 Block Diagram

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1. Pin Configuration and Functions

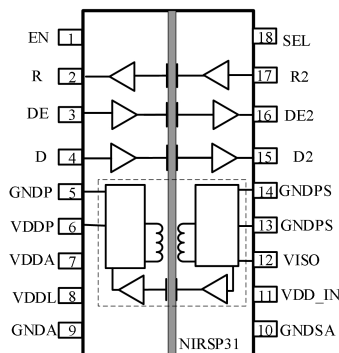


Figure 1.1 NIRSP31 Package

Table1.1 NIRSP31 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	EN	Power enable. When tied to VDDL pin or floating, the VISO output voltage is active. When a logic low voltage is applied, the VISO output voltage is shut down.
2	R	Logic Output R
3	DE	Logic Input DE
4	D	Logic Input D
5	GNDP	Isolator Side 1 Ground 1, the ground reference for VDDP
6	VDDP	Power Supply for Isolator Side 1
7	VDDA	Power Supply for Isolator Side 1
8	VDDL	I/O Power Supply input. Side1 I/O logic level.
9	GNDA	Isolator Side 1 Ground 2, the ground reference for VDDL and VDDA
10	GNDSA	Isolator Side 2 Ground 2, the ground reference for VDDIN
11	VISO_IN	Secondary Supply Voltage Input for Internal Load. This pin must be connected externally to VISO .
12	VISO	Secondary Supply Voltage Output for External Load.
13	GNDPS	Isolator Side 2 Ground 2, the ground reference for VISO
14	GNDPS	Isolator Side 2 Ground 2, the ground reference for VISO
15	D2	Logic Output D
16	DE2	Logic Output DE
17	R2	Logic Input R
18	SEL	VISO output voltage select, VISO=5V when SEL pull up to VISO or floating, VISO=3.3V when SEL pull low.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD	-0.5		6.5	V	
Maximum Input Voltage	DE,D,R2	-0.4		VDD+0.4 V _{ISO} +0.4	V	
Maximum Output Voltage	DE2,D2,R	-0.4		VDD+0.4 V _{ISO} +0.4	V	
Common-Mode Transients	CMTI	±50			kV/us	
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-40		105	°C	
Storage Temperature	T _{stg}	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD	4.5		5.5	V
Operating Temperature	T _{opr}	-40		105	°C
High Level Input Voltage	V _{IH}	0.7*VCC		VCC	V
Low Level Input Voltage	V _{IL}	0		0.3*VCC	V
Data rate	DR			20	Mbps

4. Thermal Information

Parameters	Symbol	QFN18	Unit
IC Junction-to-Air Thermal Resistance	θ _{JA}	56.8	° C/W
Junction-to-case (top) thermal resistance	θ _{JC (top)}	15.6	° C/W
Junction-to-board thermal resistance	θ _{JB}	28.5	° C/W

5. Specifications

5.1. Isolated DC/DC Converter Static Specifications

(VDD=4.5V~5.5V, SEL=VISO, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	V _{ISO}	4.75	5	5.25	V	
Line Regulation	V _{ISO(LINE)}			2	mV/V	
Load Regulation	V _{ISO(LOAD)}		0.4	5	%	
Output Ripple	V _{ISO(RIP)}		90		mVpp	
Output Noise	V _{ISO(NOISE)}		200		mVpp	
Efficiency at maximum load current	EFF		47		%	
Output supply current	I _{ISO}			60	mA	
VDD supply current without digital isolator	I _{VDD_POWER}		13		mA	No VISO Load
				173	mA	Full VISO Load (I _{ISO} =100mA)
Thermal Shutdown Temperature			154		°C	

(VDD=4.5V~5.5V, SEL=VISO, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Isolated Supply Voltage	V _{ISO}	3.135	3.3	3.465	V	
Line Regulation	V _{ISO(LINE)}			2	mV/V	
Load Regulation	V _{ISO(LOAD)}		0.6	5	%	
Output Ripple	V _{ISO(RIP)}		60		mVpp	
Output Noise	V _{ISO(NOISE)}		117		mVpp	
Efficiency at maximum load current	EFF		39		%	
Output supply current	I _{ISO}			60	mA	
VDD supply current without digital isolator	I _{VDD_POWER}		11		mA	No VISO Load
			134		mA	Full VISO Load (I _{ISO} =100mA)
Thermal Shutdown Temperature			165		°C	

5.2. Digital Isolator Electrical Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDDPOR		4.3		V	POR threshold as during power-up
	VDD HYS		0.4		V	POR threshold Hysteresis

High Level Input Voltage	VIH	0.7*V _{DD}			V	DE,D,R2
Low Level Input Voltage	VIL			0.3*V _{DD}	V	DE,D,R2
High Level Output Voltage	VOH	0.8V _{DD}			V	IOH ≥ -4mA
Low Level Output Voltage	VOL			0.2V _{DD}	V	IOL ≤ 4mA
Output Impedance	R _{out}		50		ohm	
Input Pull high Current	I _{pullup}		8	25	uA	DE
Input Pull low Current	I _{pulldown}	-25	-8		uA	EN,D,R2,SEL
Common Mode Transient Immunity	CMTI	50			kV/us	

(V_{DD}=4.5V~5.5V, SEL=VISO, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at V_{DD} = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD} (Q0)		10.56		mA	All Input 0V
	I _{DD} (Q1)		14.61		mA	All Input at supply
	I _{DD} (20M)		17.15		mA	All Input with 20Mbps, C _L =15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW				ns	
Propagation Delay	t _{PLH}		44	60	ns	
	t _{PHL}		44	60	ns	
Pulse Width Distortion	PWD			5.0	ns	t _{PHL} - t _{PLH}
Rising Time	tr			5.0	ns	C _L = 15pF
Falling Time	tf			5.0	ns	C _L = 15pF
Channel-to-Channel Delay Skew	t _{sk} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{sk} (p2p)			5.0	ns	

(V_{DD}=4.5V~5.5V, SEL=GND, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at V_{DD} = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD} (Q0)		10.21		mA	All Input 0V
	I _{DD} (Q1)		11.65		mA	All Input at supply
	I _{DD} (1M)		15.21		mA	All Input with 20Mbps, C _L =15pF
Data Rate	DR	0		20	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}		44	60	ns	

	t_{PHL}		44	60	ns	
Pulse Width Distortion	PWD			5.0	ns	$ t_{PHL} - t_{PLH} $
Rising Time	t_r			5.0	ns	$C_L = 15\text{pF}$
Falling Time	t_f			5.0	ns	$C_L = 15\text{pF}$
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

5.3. Typical Performance Characteristics

5.4. Parameter Measurement Information

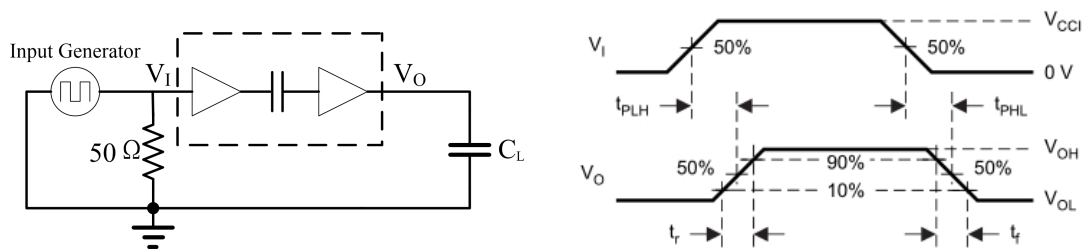


Figure 5.7 Switching Characteristics Test Circuit and Waveform

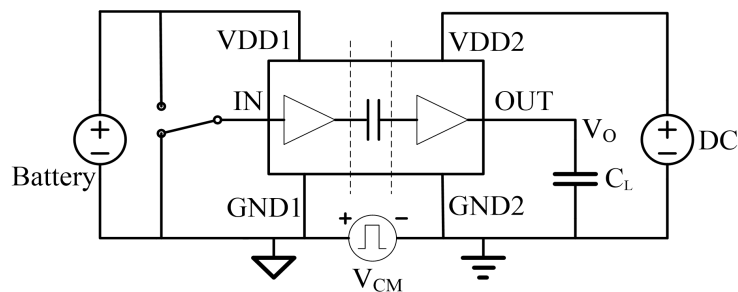


Figure 5.8 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>value</i>	<i>unit</i>	<i>comments</i>
Minimum External Air Gap (Clearance)	L(I01)	2.5	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	2.5	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II		

7. Function Description

The NIRSP31 devices are value line triple-channel digital isolators with integrated isolated DC-DC converter. The digital isolators are based on Novosense capacity isolation barrier technique. The isolated DC-DC converter provide up to 300mW output power use on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on capacity isolation technology. The NIRSP31 device are safety certified by UL1577 support $2kV_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NIRSP31 is up to 20Mbps, and the common-mode transient immunity (CMTI) is up to 50kV/us. The logical level of digital isolators on left side can be set by VDDL pin which can support the application when the supply voltage and I/O voltage level are different.

The high integrated solution can help to simplify system design and improve reliability. The NIRSP31 devices are suitable for the limited PCB space applications. The devices are also suitable for wide temperature application which the most the power module can not support.

7.1. Device Functional Modes

The NIRSP31 devices provide 5V to 5V, 5V to 3.3V conversion mode, the output voltage can be set by SEL pin. Supply configuration table showed below.

<i>SEL PIN</i>	<i>VDD</i>	<i>VISO</i>
Shorted to VISO or floating	5V	5V
Shorted to GND2	5V	3.3V

The NIRSP31 devices provide four channel digital isolators. The digital isolators have default output status when VDDIN is unready and VDDOUT is ready as shown in below table.

<i>Input</i>	<i>VDDIN status</i>	<i>VDDOUT status</i>	<i>Output</i>	<i>Comment</i>
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	H	The output follows the same status with the input within 60us after input side VDDIN is powered on.

7.2. EMI Considerations

The NIRSP31 devices are using on chip transformer, so the power transfer must operate at high frequency allow higher efficiency transfer using the small transformer. This will cause emissions which need to pay attention to PCB layout if the application allow low emission. Please see the application note if needed.

7.3. Output Short and Over Temperature Protection

The NIRSP31 devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transfer power will be limited. So the temperature of the device will be low, and the device is protected.

The NIRSP31 devices are also protected against over temperature. When the devices detect the chip is over 165°C, the device will be shut down until the temperature of the device is below 145°C.

8. Application Note

8.1. Typical Application

The NIRSP31 requires a 0.1 μF and 10uF bypass capacitors between VDD and GND1, VISO and GND2. The capacitor should be

placed as close as possible to the package. This is very important for the performance of the device. The figure8.1 is the figure8.2 is the typical isolated RS485 schematic using NIRSP31.

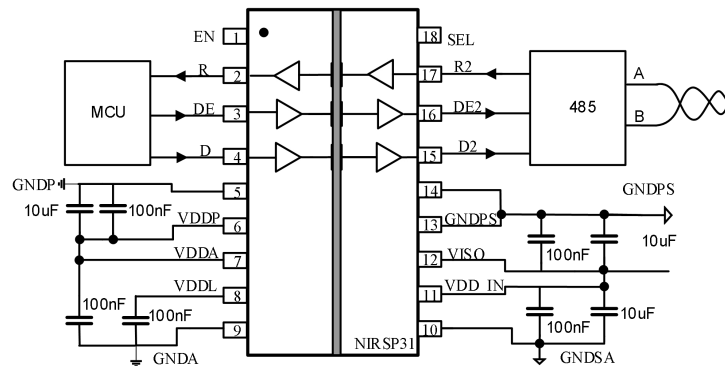


Figure8.1 Isolated RS485 schematic using NIRSP31

8.2. PCB Layout

The low ESR capacitors should be connected between Pin 5 (GNDP) and Pin 6 (VDDP) and Pin 7 (VDDA), Pin 8 (VDDL) and Pin 9 (GND1) for VCC. The VISO and VDDIN capacitors are connected between Pin 10 (GNDSA) and Pin 11 (VDDIN) and Pin 12 (VISO) and Pin 13 (GNDPS). To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required with the smaller of the two capacitors located closest to the device. The recommended capacitor values are 0.1 μ F and 10 μ F for VDDP at Pin 5 and Pin 6 and VISO at Pin 12 and Pin 13. Capacitor values of 0.01 μ F and 0.1 μ F are recommended for VDDIN at Pin 10 and Pin 11 and VDDL&VDDA at Pin 7&8 and Pin 9. The recommended best practice is to use a very low inductance ceramic capacitor, or its equivalent, for the smaller value capacitors. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 10 mm.

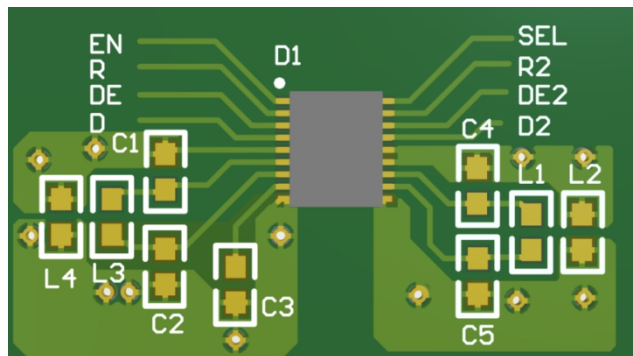


Figure8.2 Recommended PCB Layout — Top Layer

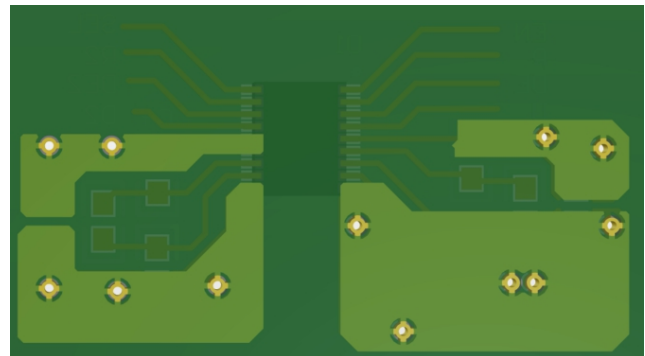


Figure8.3 Recommended PCB Layout — Bottom Layer

9. Package Information

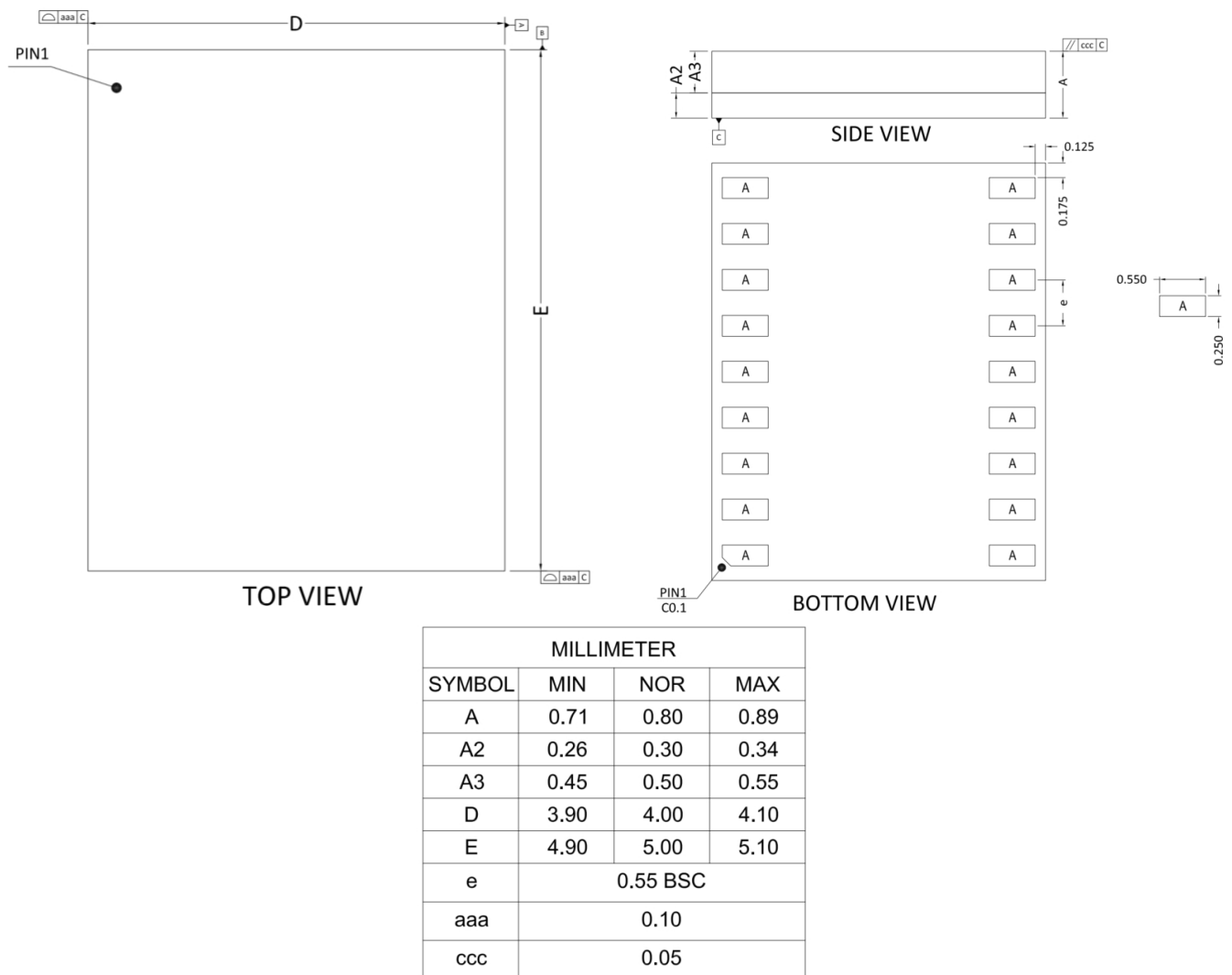


Figure 9.1 LGA18 Package Shape and Dimension in millimeters

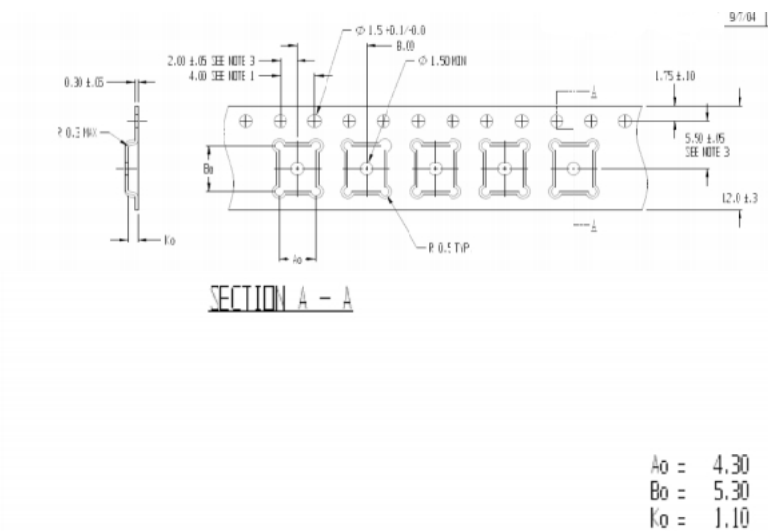
10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NIRSP31-DLARR	2	2	1	20	-40 to 105°C	3	LGA18	LGA18	2500

11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NIRSP31	Click here	Click here	Click here	Click here

12. Tape and Reel Information



- NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
 2. CARBER IN COMPLIANCE WITH EIA-481
 3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

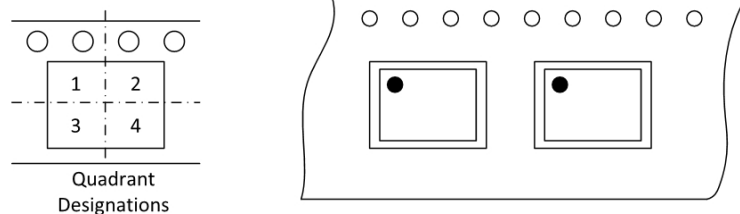


Figure 12.1 Tape and Reel Information of QFN18

13. Revision History

Revision	Description	Date
0.0	Original	2020/12/1
0.1	Changed spec value	2021/3/1
0.2	Added tape and reel information	2021/6/23
0.3	Modified application circuit	2021/6/25
0.4	Modified part number	2021/7/6